ABSTRACT OF THE DISCLOSURE

A process for patterning dielectric layers of the type typically found in optical coatings in the context of MEMS manufacturing is disclosed. A dielectric coating is deposited over a device layer, which has or will be released, and patterned using a mask layer. In one example, the coating is etched using the mask layer as a protection layer. In another example, a lift-off process is shown. The primary advantage of photolithographic patterning of the dielectric layers in optical MEMS devices is that higher levels of consistency can be achieved in fabrication, such as size, location, and residual material stress. Competing techniques such as shadow masking yield lower quality features and are difficult to align. Further, the minimum feature size that can be obtained with shadow masks is limited to ~100 μm, depending on the coating system geometry, and they require hard contact with the surface of the wafer, which can lead to damage and/or particulate contamination.